INTERMODULATION DISTORTION SIMULATION USING PHYSICAL GaAs FET MODEL

W. Contrata, Y. Ando, *Y. Hori, and M. Kuzuhara

NEC Corp. System Devices and Fundamental Res. *System ULSI Development Division
2-9-1 Seiran, Otsu, Shiga 520-833, Japan contrata@pwd.cl.nec.co.jp

Abstract — **Intermodulation distortion is simulated using a physical GaAs FET model for the first time, to our knowledge. A GaAs FET power amplifier, including input and output circuits, is examined. For the FET, a fully 2-dimensional Monte Carlo simulator is used. The simulated P_{IN}-P_{OUT} performance is in fair agreement with measured data. Gain and phase compression (AM-PM) characteristics are simulated, and correlated to features in the RF I-V characteristics. Finally, third order intermodulation distortion is estimated from the AM-PM characteristics and compared to measurement, with qualitative agreement. This technique advances the art of computer aided design of nonlinear devices because it allows the prediction of distortion characteristics before undertaking an expensive and time-consuming device fabrication.**

I. INTRODUCTION

Large signal device simulation of FETs is typically performed using empirical models. Highly accurate models over a wide range of bias and power level are required to reproduce distortion characteristics for digital systems. This has led to models with a large number of parameters, whose values are difficult to determine and whose physical significance is unclear. When successful, these empirical models are useful for reproducing device behavior, but not for optimizing device structures. On the other hand, physical modeling uses parameters with clear significance and has potential for optimization. Physical, quasi-2-dimensional device/circuit simulators have made great advances recently, including prediction of power performance with harmonics, and achieving commercial introduction [1]. However, distortion predictions have not been reported yet, and even more accurate simulation technology is desirable. The purpose of this work is to demonstrate intermodulation distortion simulation of a GaAs FET amplifier using a fully 2-dimensional Monte Carlo device model.

II. METHOD

A power amplifier based on the GaAs FET shown in Fig. 1 was simulated. The channel layer doping and thickness were 2×10^{17} cm^{-3} and 120 nm, respectively. A double recess structure was employed with a 500 nm long gate centered in a 1600 nm wide first recess. The depth of the narrow second recess was 30 nm into a 100 nm thick undoped GaAs Schottky layer. This kind of structure can achieve high breakdown voltage due to the wide recess and undoped Schottky layer, as well as reduced surface effects due to the narrow second recess.

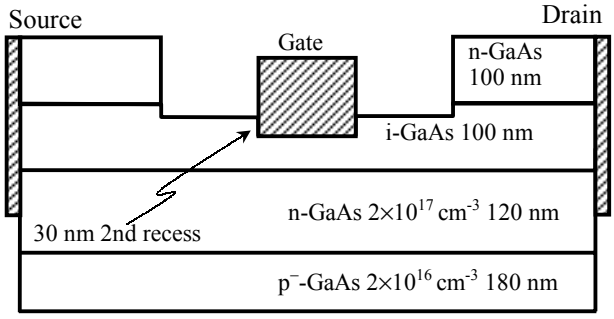

Fig. 1 GaAs FET structure.

The GaAs FET was modeled using a 2-dimensional Monte Carlo (MC) simulator [2]. The conduction band was analytically approximated by 3 valleys, including nonparabolicity. Scattering due to polar optical and inter-valley phonons and ionized impurities were included. Approximately 18000 superparticles were simulated, and the field update time (Δt) was 2 fs. This model includes forward gate current due to electrons entering the gate, but not reverse gate current due to electrons leaving the gate or holes. Currents were normalized for a gate width

of 1 mm. Simulated DC I-V characteristics are shown in Fig. 2. Although the simulation reproduced the measured (not shown) maximum drain current (I_D) well, the pinch-off voltage of -3.5 V was more negative than the measured value of -2.8 V. Thus the simulated transconductance is low. This probably indicates that the fabricated and nominal structures were different.

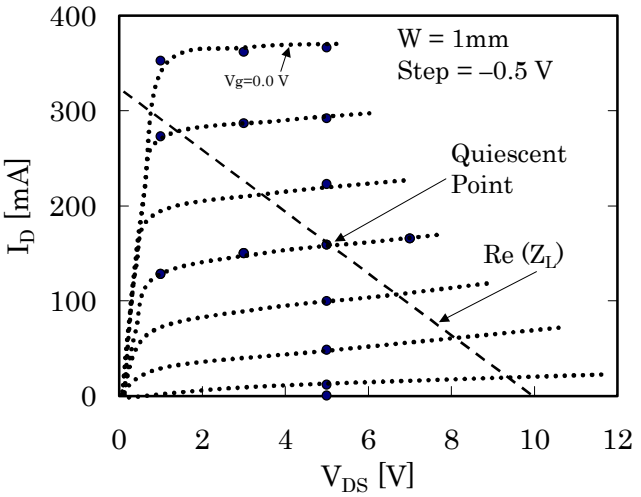

Fig. 2 Simulated I-V characteristics, with quiescent bias point and real part of load line.

Based on simulated GaAs FET small signal characteristics and DC characteristics, a power amplifier with one-stage LC matching networks was designed (Fig. 3). Experimentally determined device parasitic elements were included in the circuit. A feedback network was added for improved stability. The quiescent point was a drain-source bias (V_{DS}) of 5.0 V and gate-source bias (V_{GS}) of -1.5 V. The real part of the load impedance (Z_L) was set to 25 Ω at 10 GHz for large current and voltage swing (see Fig. 1). The source impedance (Z_S) and the imaginary part of Z_L were chosen for maximum small signal gain. The DC drain bias was explicitly included with an inductor for RF isolation, and the gate voltage bias was included in the signal source. Instead of a blocking capacitor at the output, a power supply prevented the flow of DC current through the output resistor. The system impedance (Z_0) was 50 Ω.

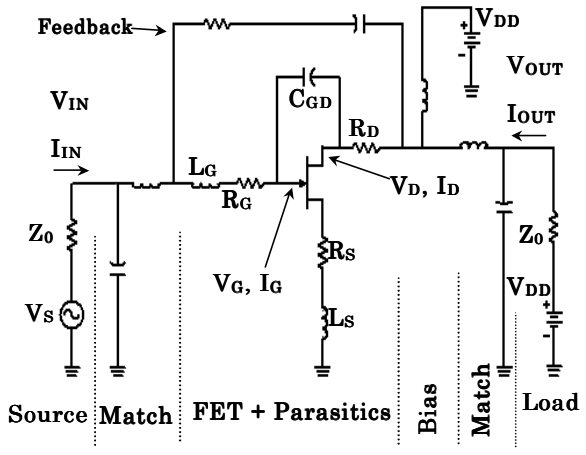

Fig. 3 Simulated power amplifier circuit.

The circuit was modeled by discretizing Kirchhoff's laws with time step Δt (the MC field update time), and the resulting equations were solved by Gaussian elimination. Device and circuit models were coupled in a straightforward way at the device terminals. The terminal voltages were boundary conditions for the MC, and the currents are boundary conditions for the circuit. Device and circuit problems were solved sequentially, as shown in the flow chart in Fig. 4. The gate, drain, and

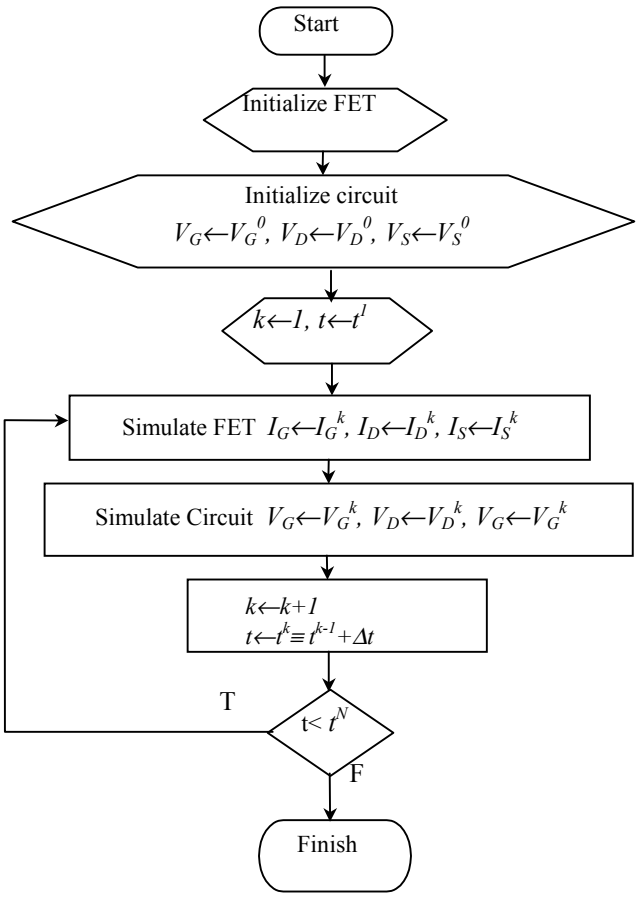

Fig. 4 Flow chart for coupled device/circuit simulation.

source biases are set to their initial values, V_G^0, V_D^0, and V_S^0, respectively. Here the superscript denotes time step number. The biases are passed to the MC, which calculates the resulting terminal currents for the time step 1 ($t^1 \equiv \Delta t$): I_G^1, I_D^1, and I_S^1. These currents are passed to the circuit simulator, which calculates the terminal biases: V_G^1, V_D^1, and V_S^1. These are passed back to the MC, which calculates the currents for step 2 ($t^2 \equiv 2\Delta t$). The process repeats until the final time step t^N is reached.

The simple circuit-device model described above is prone to oscillation because the circuit and device simulations are sequential rather than simultaneous. In other words, the model is not self-consistent on the time scale Δt. Oscillations may be avoided by anticipating the FET response to bias changes while performing the circuit calculation. At the time scale Δt, this response is dominated by capacitance, because the electron density and average velocity hardly change. This high frequency capacitance was extracted from the MC and incorporated in the circuit.

The amplifier was simulated in the time domain with input power (P_{IN}) of −20 to 27 dBm at 10 GHz for 10 periods (1 ns) or longer. Typical input and output current and voltage levels (I_{IN}, V_{IN}, I_{OUT}, V_{OUT}, defined in Fig. 3) are shown in Fig. 5. The first five periods show transient effects and were omitted from subsequent analysis. The remaining data were used to calculate the output power (P_{OUT}), gain (G), and power added efficiency (PAE) at the fundamental frequency.

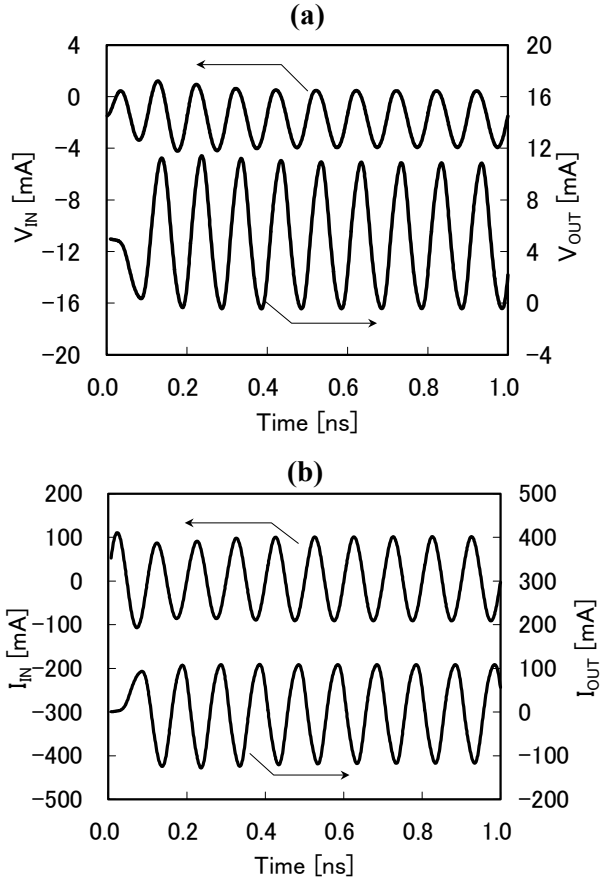

Fig. 5 Simulated a) voltage and b) current wave forms at the source (V_{IN}, I_{IN}) and load (V_{OUT}, I_{OUT}). The input and output power at the fundamental frequency (10 GHz) and the amplitude (AM) and phase (PM) modulation characteristics are determined from these data.

III. Results And Discussion

The resulting P_{OUT}, G, PAE, and I_G characteristics are shown in Fig. 6, along with measured data. Fair agreement was achieved, but the simulated G and PAE were lower than measured data, possibly due to the transconductance discrepancy mentioned above. Also, at high input levels, simulated I_G rises more sharply than measured I_G. Fig. 7 shows simulated gain and phase distortion (AM-PM), and Fig. 8 shows simulated RF I-V characterististics for various P_{IN}, superimposed on the DC characteristic. Gain compression was weak for P_{IN}<12 dBm and strong higher P_{IN} (Fig. 7). The transition occurs when the

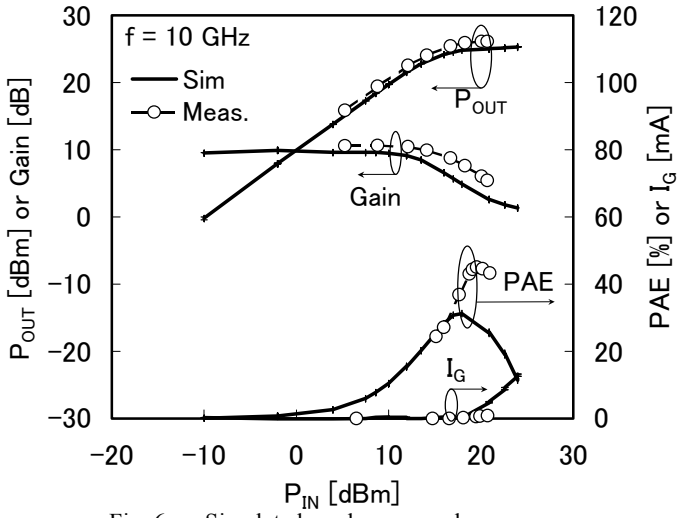

Fig. 6 Simulated and measured power characteristics

RF I-V characteristic approaches the zero drain current axis (Fig. 8, P_{IN}=11.9 dBm). AM-PM characteristics show a slight decrease in phase starting at P_{IN}=12 dBm and a strong increase from P_{IN}=18 dBm. The latter corresponds to increasing forward gate current. Finally, the AM-PM characteristics were used to predict 2-Tone performance [3]. The results are shown in Fig. 9, along with measured data from an HFET with similar power handling capability. Qualitative agreement is good. IM3 shows a strong increase above P_{OUT}=10 dBm. Further investigation showed that effect of phase distortion on IM3 was negligible in this case.

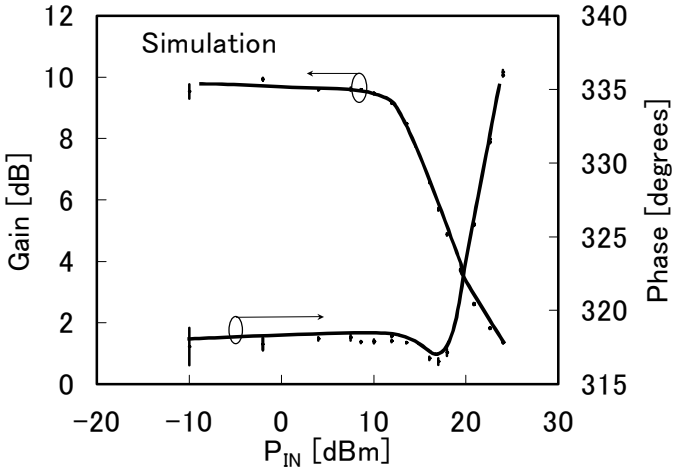

Fig. 7 Simulated gain and phase distortion characteristics.

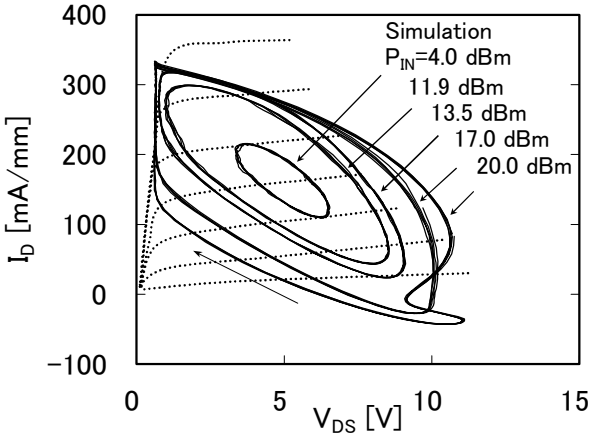

Fig. 8 Simulated RF I-V characteristics for various P_{IN}, superimposed on DC characteristic.

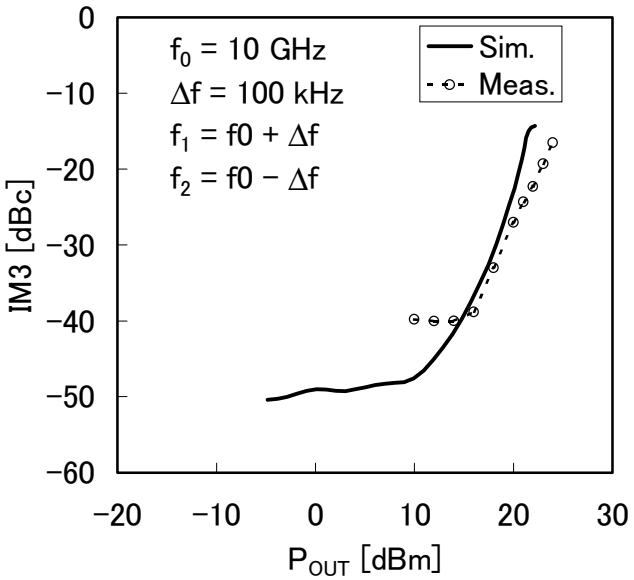

Fig. 9 Simulated and measured IM3.

IV. Conclusion

The technique described above advances the art of computer aided design of nonlinear devices because it enables optimization of device and circuit for commercially important specifications, like IM and ACPR, from physically accurate numerical simulations. Although this technique requires long calculation times (about 2 days for each point of Fig. 6 on a Pentium 3 at 600 MHz), it is inexpensive compared to a device fabrication.

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